DAVICOM Semiconductor, Inc.

DM9625I

USB to UART converter

DATA SHEET

Version: DM9625I-11-MCO-DS-P01

March 16, 2022

Content

1. General Description

The DM9625I provides highly compatible USB drivers to simulate the traditional COM port (via virtual COM Port) on most operating systems allowing existing serial UART applications based on legacy COM port to easily migrate and be made USB ready. The DM9625I provides an advanced full-featured single-chip bridge solution for connecting a full-duplex UART asynchronous serial interface device to any Universal Serial Bus (USB) capable host.

DM9625I also integrates an internal precise clock generator (or optional external crystal), USB transceiver, LDO voltage regulator, power-on-reset (POR), FIFO data buffers, and OTP.

2. Features

USB Interface

- Fully compliant with USB2.0 (Full-speed mode)
- UHCI/OHCI (USB1.1), EHCI (USB2.0), xHCI (USB3.1) Host controller compatible
- Highly integrated USB1.1 FS transceiver with integrated termination resistors
- CDC-ACM support
- Integrate 256-byte OTP for USB device descriptors and GPIO custom configuration and support 128- or 256-byte external EEPROM for USB device descriptors
- Each IC has unique serial number (ID) stored in OTP
- Supports bus-power, self-power and high-power USB device configuration
- Supports Windows USB Selective Suspend (Remote Wakeup enabled)
- Supports VBUS input detect function to attach USB host after VBUS is detected
- Supports 3.3V VBUS voltage operation

GPIO Interface

- Versatile GPIO functions and routing logic provides easy to use multi-IO functions
- Configurable I/O pin output driving strength
- Total 8 General Purpose I/O (GPIO) pins can be used after configured
- Optional Clock output to external MCU

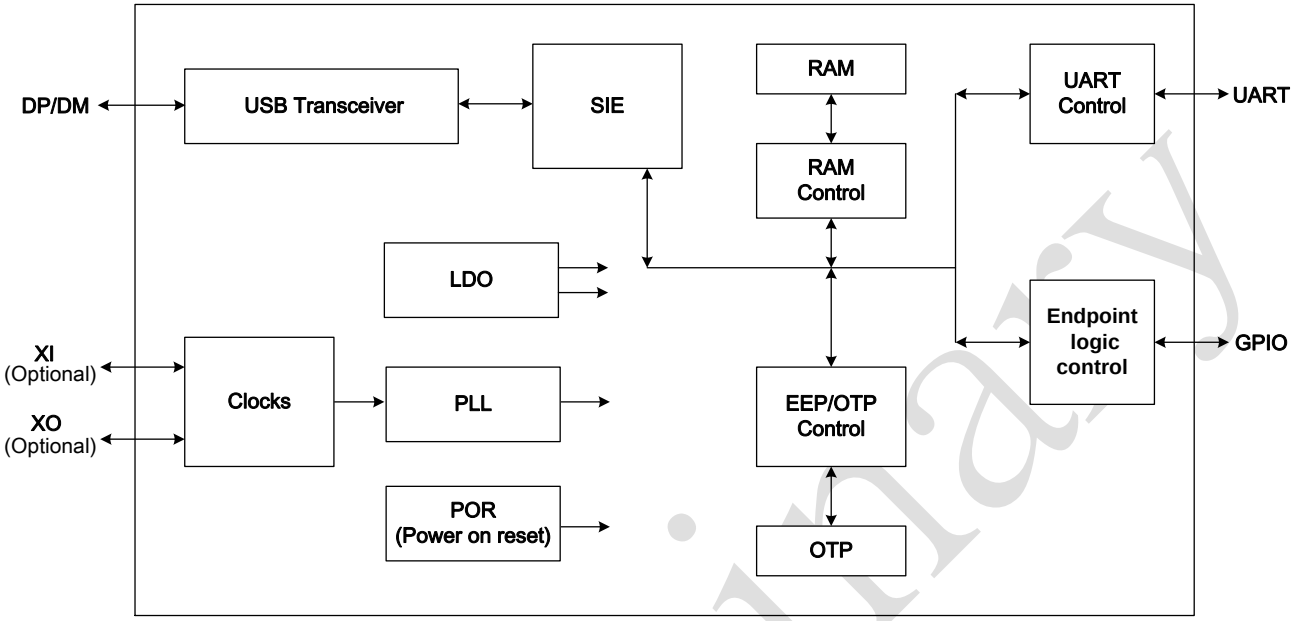
UART Interface

- Supports Serial UART Interface:
  - RS232, RS422, RS485
  - Flexible baud rate support from 300 to 12Mbps
  - 5, 6, 7 or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and a half, or two stop bits
  - Hardware flow control (CTS/RTS and/or DSR/DTR)
  - Software flow control (XON/XOFF)
  - Multidrop mode (RS422, RS485)
  - Auto RS-485 Half-Duplex Control
  - Configurable Remote Wakeup pin
- 1024-byte FIFO buffers
- Configurable Transmit and Receive LED pins
- Suspend pin control for RS232 transceiver
- UART inverted signal configurable option

Miscellaneous

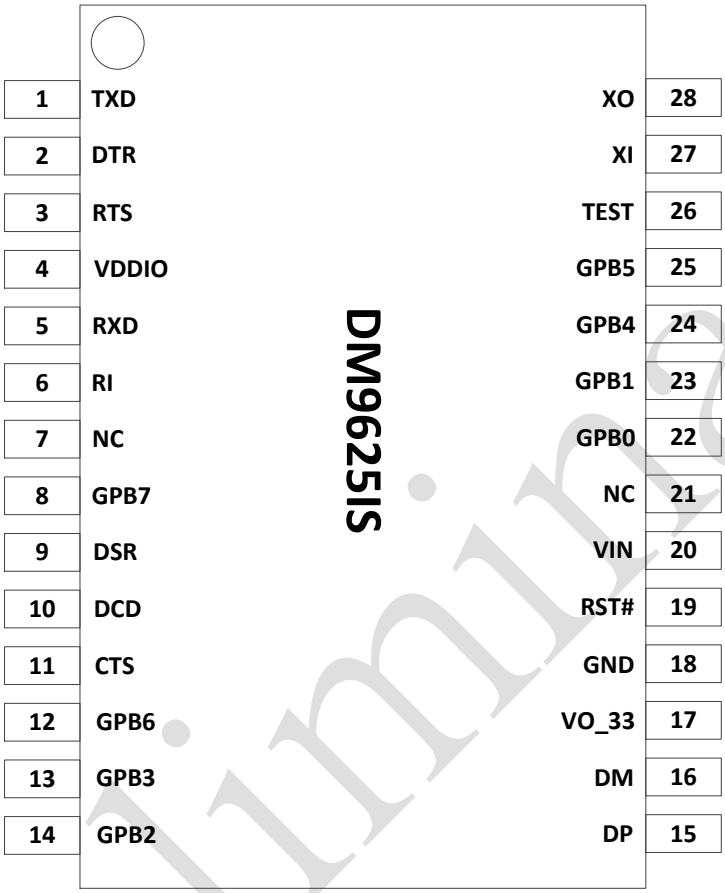
- Integrated self-generated precise clock generator
- Integrated Power-on-Reset (POR) circuit
- Integrated 5V to 3.3V LDO than can support 80mA for external components
- 3.3V brown out detector to reset chip and detach USB
- Low operating power and USB suspend current
- Wide I/O voltage range (1.8V/2.5V/3.3V and 5V tolerance)
- -40℃ to +85℃ operating temperature
- 28-pin SSOP and 8-pin SOP package (RoHS compliant and Pb-free Green compound)

3. Block Diagram

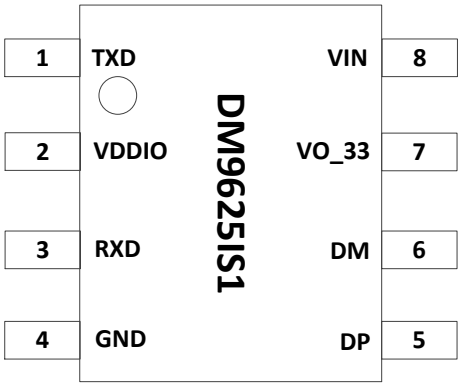


4. Pin Configuration

4.1. SSOP 28-Pin Package



4.2. SOP 8-PIN Package



5. Pin Out Description

5.1. USB Pins

Pin Name	SSOP28	SOP8	Type	Description
DP	15	5	I/O	USB Port Data Plus (D+) Signal
DM	16	6	I/O	USB Port Data Minus (D-) Signal

5.2. UART Pins

Pin Name	SSOP28	SOP8	Type	Description
TXD	1	1	O	Serial Port Transmitted Data Output
DTR	2	--	I/O	Serial Port Data Terminal Ready Control Output
RTS	3	--	I/O	Serial Port Request to Send Control Output
RXD	5	3	Input, PU	Serial port Received Data Input
RI	6	--	Input	Serial Port Ring Indicator Control input
DSR	9	--	I/O	Serial Port Data Set Ready Control Input
DCD	10	--	I/O	Serial Port Data Carrier Detect Control Input
CTS	11	--	I/O	Serial Port Clear To Send Control Input

5.3. Configurable GPIO Pins – Group B

Pin Name	SSOP28	SOP8	Type	Description
GPB0	22	--	I/O	Configurable GPIO Pin.
GPB1	23	--	I/O	Configurable GPIO Pin.
GPB2	14	--	I/O	Configurable GPIO Pin. Factory default is EEPROM SDA open-drain pin
GPB3	13	--	I/O	Configurable GPIO Pin. Factory default is EEPROM SCL open-drain pin
GPB4	24	--	I/O	Configurable GPIO Pin.
GPB5	25	--	I/O	Configurable GPIO Pin.
GPB6	12	--	I/O	Configurable GPIO Pin. Factory default is SUSPN serial port output pin
GPB7	8	--	I/O	Configurable GPIO Pin. Factory default is TXEN serial port output pin

5.4. Power and Ground Pins

Pin Name	SSOP28	SOP8	Type	Description
VDDIO	4	2	Power	+1.8V to +3.3V I/O signal power input pin
VO_33	17	7	Power	+3.3V output power from integrated LDO regulator.
NC2	21			No connection
NC1	7			No connection
GND	18	4	Power	Ground
VIN	20	8	Power	USB port VBUS input power supply. For self-powered design, supply +3.3V to this pin.

5.5. Miscellaneous Pins

Pin Name	SSOP28	SOP8	Type	Description
RST#	19	--	Input, PU	Active low Reset pin. Internal pull-high to VDDIO.
XI	27	--	Input	Optional 12 Mhz crystal oscillator input. If not used, leave pin floating.
XO	28	--	Output	Optional 12 Mhz crystal oscillator output. If not used, leave pin floating.
TEST	26	--	Input, PD	Test mode, active high. Internal pull-low. (For normal operation, connected to GND)

6. Pin Mode

SSOP28 pin #	M0	MX
1	TXD	TXD
2	DTR	DTR
3	RTS	RTS
5	RXD	RXD
6	RI	RI
8	GPB7	GPB7
9	DSR	DSR
10	DCD	DCD
11	CTS	CTS
12	GPB6	GPB6
13	GPB3	GPB3
14	GPB2	GPB2
19	RST#	RST#
22	GPB0	=1
23	GPB1	GPB1
24	GPB4	=0
25	GPB5	=0
26	TEST=0	=1

Note:
1. M0: normal mode(TEST=0) (note : use internal 12MHz oscilator)
2. MX mode to used external 12MHz crystal from XI/XO pin:
   TEST pin connect to high
   GPB0 pin connect to high.
   GPB4 pin connect to ground.
   GPB5 pin connect to ground

7. Function Description

7.1. USB Transceiver

The USB Transceiver compliant with USB 2.0 Full Speed mode. It internally builds about 1.5K pull-up resistor in DP pin and series termination resistors on the DP and DM data lines.

7.2. SIE

The USB full speed Serial Interface Engine. It include RX (DPLL, serial to parallel), TX (8-bit parallel to serial), Suspend/Wakeup, EP0 (Control packet), EP1 (Bulk IN), EP2 (Bulk OUT), and EP3 (interrupt) function.

7.3. RAM and RAM Control

There are 1K bytes internal SRAM and its control logics for USB Bulk IN/OUT transfer and UART TX/RX FIFO.

7.4. OTP and EEPROM/OTP Control

There are 256 bytes internal OTP (One Time Program-ROM) and external 128 or 256 bytes EEPROM I2C interface for USB string descriptors and GPIO configurations. The more detailed GPIO configuration is described in EEPROM/OTP writer user manual document. Also see Sec. 7.9 GPIO Multi-Function for detailed.

7.5. UART Control

The control logic for UART TX (Bulk OUT to TXD pin) and RX (RXD pin to Bulk IN) functions.

7.6. Endpoint Logic Control

The USB Endpoint control and status functions to process Endpoint control packets to control GPIO pins functions like UART TX/RX LED, clock output, suspend wakeup, and EEPROM I2C interface.

7.7. Clocks and PLL

This block implements 12MHz crystal oscillator (in MX mode) and internal RC oscillator (in M0 mode) to generate 48MHz PLL clock for USB SIE and UART control logics.

7.8. LDO and internal Power-On Reset

This block implements USB VIN 5V to 3.3V LDO and also generate internal Power-on Reset (in M0 mode) combined with RSTB pin to initialize internal USB and UART control logics. It also provides 3.3V brownout detection output (BOD) to reset chip and detached USB connection.

7.9. GPIO Multi-Function Options

GPIO	SSOP28	(mode=0)	(mode=1)	(mode=2)	(mode=3)
GPA_0	1	TXD	TXD	TXD	TXD
GPA_1	5	RXD	RXD(WAKEUP)	RXD	RXD
GPA_2	3	RTS	TX_LED	CLK_OUT	SUSPN
GPA_3	11	CTS	RX_LED	TRX_LED	WAKEUP
GPA_4	2	DTR	TX_LED	CLK_OUT	EE_SDA
GPA_5	9	DSR	RX_LED	TRX_LED	EE_SCL
GPA_6	10	DCD	VBUS_DET	USB_CFG	TXEN
GPA_7	6	RI	RI (WAKEUP)	RI	RI
GPB_0	22	GPIO0	TX_LED	CLK_OUT	TXEN
GPB_1	23	GPIO1	RX_LED	TRX_LED	TX_LED
GPB_2	14	GPIO2	VBUS_DET	EE_SDA	USB_CFG
GPB_3	13	GPIO3	USB_CFG	EE_SCL	VBUS_DET
GPB_4	24	GPIO4	CLK_OUT	RX_LED	TRX_LED
GPB_5	25	GPIO5	VBUS_DET	WAKEUP	TXEN
GPB_6	12	SUSPN	GPIO6	WAKEUP	CLK_OUT
GPB_7	8	TXEN	GPIO7	SUSPN	USB_CFG

Note:

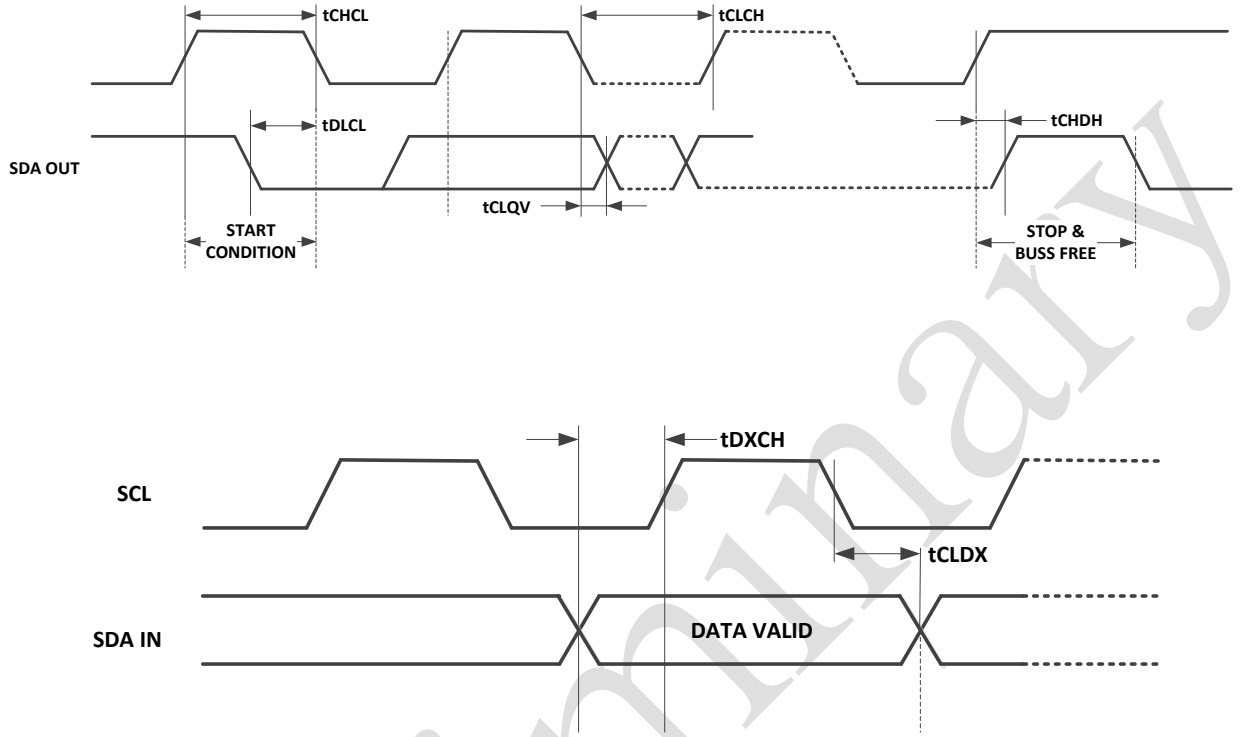
1. WAKEUP event sources:
   GPA1(RXD), GPA_3 (CTS) and GPA_7 (RI) are active low
   GPB5 and GPB6 are active high.
2. The WAKEUP priority is:
   GPA_7 (RI mode 1) > GPA_1 (RXD mode 1) > GPA_3 (mode 3)
   > GPB_5 (mode 2) > GPB_6 (mode 2) > GPA_7 (RI mode 0,2,3)
   When they are set to WAKEUP function at the same time, only the highest priority input is active.
   For example, if GPA_1 and GPA_3 are both set as WAKEUP input, then only GPA_1 will work.
3. VBUS_DET event sources:
   GPA_6 (mode 1), GPB_2 (mode 1), GPB_3 (mode 3) and GPB_5 (mode 1) are all active high.
4. The priority of VBUS_DET is:
   GPA_6 (mode 1) > GPB_2 (mode 1) > GPB_3 (mode 3) > GPB_5 (mode 1)
   Only the highest priority input is active.
   If VBUS_DET is not configured by any pins, it is the default value “1”.
5. EEPROM (EE_SDA/EE_SCL) function pins:
   GPB_2/3 (mode 2) and GPA_4/5 (mode 3)
6. The priority of EEPROM (EE_SDA/EE_SCL) pin is GPB_2/3 (mode 2) > GPA_4/5 (mode 3)

8. DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Power						
VIN	Power Supply Voltage Range	2.8	5	5.5	V	
VDDIO	Power Supply for I/O Pins	1.8	3.3	3.63	V	
VO_33	3.3V Output of Regulator	3.1	3..3	3.4	V	
I_{DD}	Operating Current		9.5	15	mA	
I_{SUS}	Suspend Current		420	450	uA	
Inputs						
VIL	Input Low Voltage	-0.3	-	0.99	V	VDDIO=3.3V
VIH	Input High Voltage	2.3	-	5	V	VDDIO=3.3V
IIL	Input Low Leakage Current	-10		10	uA	VDDIO=3.3V
IIH	Input High Leakage Current	-10		10	uA	VDDIO=3.3V
Outputs						
VOL	Output Low Voltage	-	-	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	-	-	V	IOH = -4mA

9. AC characteristics

9.1. EEEPROM I2C interface timing



9.2. AC Characteristic

Symbol	Parameter	Min	Max	Unit
t_{CHCL}	Clock Pulse Width High	5.12	20.48	us
t_{CLCH}	Clock Pulse Width Low	5.12	20.48	us
t_{DLCL}	Input Low to Clock Low (START)	7.66	30.64	us
t_{CHDH}	Clock High to Input High (STOP)	7.7	30.8	us
t_{CLOV}	Clock Low to Next Data Out Valid	2.58	10.32	us
t_{DXCH}	Input Transition to Clock High	0.1		us
t_{CLDX}	Clock Low to Input Transition	0.1		us
f_c	Clock Frequency		100	kHz

10. Ordering Information

Part Number	Pin Count	Package
DM9625IS	28	SSOP(Pb-Free)
DM9625IS1	8	SOP(Pb-Free)

Disclaimer

The information appearing in this publication is believed to be accurate on the date it was provided and is subject to change without notice. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications.

Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards.

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6, Li-Hsin 6th Rd.,
Hsinchu Science Park,
Hsin-chu City 300, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.